REMARKS

The Office Action dated October 5, 2004 has been received and carefully considered. Withdrawn Claims 33-37 have been canceled without prejudice. Claims 38, 44 and 46 have been amended. Claims 47-49 have been newly added.

Amendments

The Cross Reference To Related Applications section has been updated as requested by the Examiner.

Claims 38, 44 and 46 have been amended to broaden their scope. For example, Claim 38 has been amended to remove the word "whether" to recite a "control signal indicating said predetermined portion of said instruction caused an exception within said coprocessor". The amendment broadens Claim 38 because after amendment the control signal is received from the coprecessor indicating the instruction caused an exception, as opposed to a possible narrower interpretation prior to amendment whereby the control signal could be interpreted as indicating the instruction caused an exception as well as indicating the instruction did not cause an exception.

Claims 47-49 have been added, and correspond to Claims 38, 44 and 46, respectfully, prior to being amended herein. Reconsideration of the outstanding rejections made by the Examiner is further respectfully requested based on the remarks below.

Indefinite Rejection of Claim 44 under 35 U.S.C. §112, second paragraph

Claim 44 has been rejected by the Office at sections 6 and 7 of the Office Action, as being indefinite for reciting "the third control signal". Upon careful review of Claim 44, the term "the third control signal" in Claim 44 is not found. Withdrawal of the §112 rejection of Claim 44 is requested pending clarification by the Examiner.

Anticipation Rejection of Claims 33-46

Claims 38-46 were rejected under 35 U.S.C. §102(b) at Sections 8 and 9 of the Office Action as being anticipated by Lee, et al. (U.S. Patent No. 4,763,242). This rejection is hereby respectfully traversed.

Claim 38, from which Claims 39-43 depend, recites providing to said coprocessor, at *least partially coincident with said decoding*: at least *a predetermined portion of said instruction, via a first portion of said coprocessor bus*. The Office states, at Section 9 of the Office Action, that Lee anticipates the emphasized elements at column 2, lines 57-63, and column 4, lines 48-68. The Applicant respectfully disagrees.

Column 2, lines 57-63 as relied upon by the Office recite:

> An SFU receives and sends data to the main processor's registers. An SFU can be incorporated into the computer by directly impacting internal register buses of the main processor. Direct coupling to the main processor's internal register buses enables an SFU to achieve a very high performance level. For an integrated main processor, such as a Very Large Scale Integrated processor on a chip, an SFU can also be incorporated by attaching to an external bus, achieving a reduced performance level, but thereby not directly impacting the internal register buses of the main processor.

Column 4, lines 48-68 as relied upon by the Office recite:

> Instruction 127 comprises a processor field 129 and an assist field 131. Control unit 115 decodes processor field 129. If processor field 129 indicates that instruction 127 is a basic instruction, processor functional unit 117 executes instruction 127, loading or storing any required operands or results in plurality of registers 119 or in memory system 111.
>
> If processor field 129 indicates that instruction 127 is an assist instruction, stores a copy of instruction 127 is stored in a register among plurality of registers 119. An instruction space and an instruction offset which indicate a memory address 161 at which instruction 127 is located are also stored in registers 119. If a data reference is specified in instruction 127, a data space and a data offset which indicate a data address are also stored in registers 119.
>
> Instruction 127 is also transferred to either SFU 107 or COP 109, and control unit 115 directs data movement defined by processor field 129. Assist field 131 includes a map field 133, which maps instruction 127 to SFU 107, to COP 109, or to another assist.

The portions of Lee relied upon by the Examiner do not disclose providing to said coprocessor, <u>at least partially coincident with said decoding: at least a predetermined portion of said instruction</u>, via a first portion of said coprocessor bus as recited in claim 38.

Claim 38 futher recites providing to said coprocessor, at *least partially coincident with said decoding*: [...] *a first control signal indicating that said instruction is being decoded by said processor via a second portion of said coprocessor bus*. The Office states, at Section 9 of the Office Action, that Lee further anticipates the emphasized elements at column 8, lines 3-8. The Applicant respectfully disagrees.

Column 8, lines 3-8 as relied upon by the Office recite:

> AINIT 602 is a signal from main processor 103 for timing and identifying "assist cycles." ADTR 604 is a signal from main processor 103 for identifying whether an assist cycle is a data transfer cycle or a command cycle. ARDY 612 is a response signal from an assist for indicating that the assist is ready to continue.

This relied upon portion of Lee not disclose <u>providing to said coprocessor, at least partially coincident with said decoding: a first control signal</u> as recited in claim 38. Accordingly, the Office Action fails to establish that Lee discloses or suggests each and every limitation of claim 38, as well as each and every limitation of Claims 39-43, at least by virtue of their dependency from Claim 38. Moreover, the claims dependent from Claim 38 recite additional limitations neither disclosed nor suggested by Lee.

Claim 44, from which Claim 45 depends, was rejected by the Office under § 102, at section 9 of the Office Action, based upon Lee for failing to teach or define above or beyond Claims 38-43 as rejected previously in the Office Action. Claim 44 recites receiving from said processor *at least a predetermined portion of said instruction* via a first portion of said coprocessor bus *and a first control signal indicating that said instruction is being decoded by said processor*, via a second portion of said coprocessor bus.

The Office fails to establish that Lee discloses the emphasized limitations at least because Lee discloses no first control signal that indicates the instruction is being decoded by said . processor as recited in claim 44. Therefore, because Lee does not discloses or suggest each and every limitation of Claim 44, as well as each and every limitation of Claim 45, based at least in virtue of its dependency from Claim 44, withdrawal of the rejection of Claims 44 and 45 is requested.

Claim 46 has been rejected by the Office under §102 based upon Lee for failing to teach or define above and beyond Claims 38-43 as rejected previously in the Office Action. Claim 46

recites limitations similar to those discussed with reference to claim 38. For the reasons discussed in the above, Lee does not anticipate Claim 46 because Lee does not disclose providing a portion of an instruction at least partially coincident with decoding the instruction or a first control signal at least partially coincident with decoding of the instruction as recited. Therefore, the Office Action fails to establish that Lee discloses or suggests each and every limitation of Claim 46. For at least this reason, withdrawal of the rejection of Claim 46 is requested.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance and request withdrawal of the rejections put forth herein. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue. The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

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Date

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